POINT OF LOAD CONVERTERS - The Topologies, Converters, and Switching Devices Required for Efficient Conversion

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Abstract
Point of load (POL) or point of use (POU) converters are emerging as the popular solution for applications in which circuits require low voltages of 3.3 V and below. The demand for these types of voltage levels stems from the requirement for lower core voltages, and it is obvious that the current capability for these converters will increase even if the power capability stays the same. This has several implications for the power-supply circuitry, including the need to route low-voltage high current around a printed circuit board. This leads to relatively large voltage drops, higher power consumption, and large PCB tracks, and could result in poor output regulation. Furthermore, converting the voltage from 48 V to 0.9 V requires a very low duty cycle, which in turn results in low efficiency. Typically, there will be several voltage levels required across a PCB card, and these could range from 5 V down to 0.9 V, resulting in the need for multi-output converters or several POL converters.

Introduction
POL has many different topologies or configurations, and as of yet there appears to be no fixed conversion strategy for stepping down from 48 V to values that could be as low as 0.9 V. Figure 1 shows a typical architecture for supplying all the required voltage levels from a single "front-end" converter. This has a typical input voltage of 48 V, which is then stepped down, with transformer isolation to several outputs, to various voltage levels. These voltages then must be distributed to the part of the circuit that requires the power, which could be hundreds of millimeters distant. Figure 2 shows the schematic of the architecture for a distributed bus with a two-step conversion process. The second-step, or POL, converter takes the distributed bus voltage and converts it to the required voltage level at the point at which the circuit consumes the highest power. With this two-step approach, the front-end converter usually steps down to a fixed output voltage of either 8 V or 12 V. However, a new trend has been to convert the distributed bus down to a

value of 3.3 V. This voltage is then distributed around the PCB, or card, to a point of load converter, which is then used to supply the final voltage. Another option is to use a fixed duty cycle, typically resulting in a fixed ratio converter of 6:1, which is reportedly optimized to give a higher efficiency (for specified conditions) at a fixed duty cycle. However, that topology is beyond the scope of this paper.
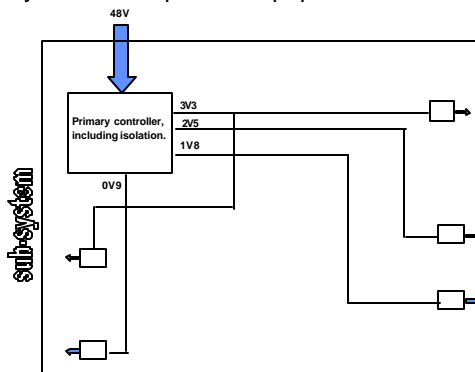

Figure 1. Block diagram showing typical architecture of a single front-end converter supplying all the voltage levels.
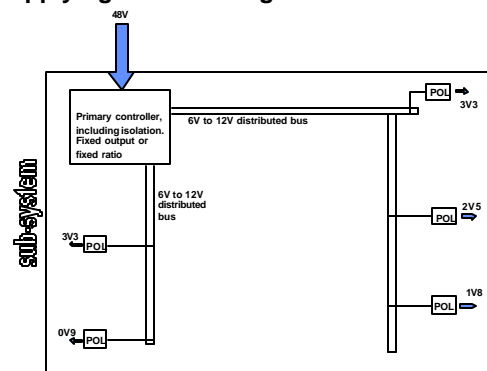

Figure 2. Block diagram showing typical architecture of a point of load (POL) distributed bus power system.

This paper explores front-end converter topologies, along with point of load converters, synchronous rectification, and the appropriate controllers and devices necessary to implement these converters. Using various semiconductor switches specifically designed for these

topologies, efficiency measurements are made and an objective assessment for these topologies in several applications and power ranges is given.

Background

Recent years have seen a move away from centralized ac-to-dc power supplies to decentralized (distributed) power systems that use dc-to-dc converters near their point of use. The major driving force has been the decrease in core voltages, and it can be seen from Table 1[1] that this trend is set to continue over the next decade. These low voltages at high currents are forcing the power conversion industry to re-evaluate conventional circuit topologies, component selection, and packaging concepts. The point of load requirement has arisen from computer hardware developments, but it is being seen throughout the semiconductor industry wherever DSPs are implemented, and it is present especially in telecom base stations and network infrastructure.

	Year							
	'01	'02	'03	'04	'05	'08	'11	'14
Process technology [μm]	0.15	0.15	0.15	0.12	0.12	0.09	0.06	0.06
Clock frequency [GHz]	1.8	21	2.5	2.9	3.5	7	11	15
Power consumption [W]	130	140	150	160	170	171	177	186
Static current requirement [A]	87	93	100	133	142	190	295	310
Min. voltage [V]	1.5-1.2	1.5-12	1.5-1.2	1.2-0.9	1.2-0.9	0.9-0.6	0.6-0.5	0.6-0.3

Table 1. Improvement in process technology and power requirements.[1]

Before the point of load converter may be considered, it is necessary to investigate the converter that provides the distributed bus. Historically, the front-end converter has always stepped down to a fixed output to supply the majority of voltages needed by the sub-system. However, with a distributed architecture, the idea is to step down to a voltage between 6 V and 12 V. This ensures that the current is large enough to necessitate the need for large busbars around the system. Now a new trend is being seen in which the distributed bus voltage is to be stepped down to 3.3 V, thus providing the 3.3-V voltage requirement directly from the front-end converter and allowing the low voltages of 2.5 V and below to be provided by a POL.

The front-end controller performs several functions, including establishing a large step-down ratio and galvanic isolation. The entire power throughput will have to pass through the front-end converter and conversely through the isolating transformer. In some circumstances this may be an off-the-shelf voltage regulator module (VRM), a custom module, or a discrete version designed in-house. Regardless of the route the manufacturer takes, the topology is usually determined by the power requirement of the system. The front-end converter must be highly efficient because all the power for the sub-system passes through it, and any inefficiency will be transferred through to the end output. For example, with a POL converter of 95% and a front-end converter of 75%, the resulting efficiency will be 71%. Therefore, great care must be taken to improve the front-end converter efficiency as much as possible.

There are several available topologies that could be considered for implementation, and Table 2 outlines several of them. Taking into consideration the power-requirement levels from Table 1, it is apparent that the forward converter, ignoring resonant topologies, is at present the most suitable topology. However, future power requirements may dictate the use of the half-bridge converter, which becomes more viable at higher power levels. This paper describes briefly both the half-bridge and forward converters, available from Vishay Siliconix, and presents efficiency results for the forward converter.

Topology	Common Characteristics				
	Power Level [W]	Voltage Stress [V]	Output Ripple Freq [Hz]	Max. Duty Cycle	Relative Cost
Flyback	5-150	$V_{in}+(N_p/N_s)V_{out}$	f_s	<0.5	Low
Forward	10-250	$2 \times V_n$	f_s	<0.5	Low
Push-Pull	15-150	$2 \times V_n$	$2 \times f_s$	<1.0	Med
Half Bridge	50-400	V_{in}	$2 \times f_s$	<1.0	Med
Full Bridge	200-2k	V_{in}	$2 \times f_s$	<1.0	High

Table 2. Characteristics of common converters.[1]

The Half-Bridge Converter[2]

The half-bridge dc-to-dc converter configuration consists of two large, equal capacitors connected in series across the dc input, providing a constant potential of ½ V_n at their junction, as shown in Figure 3. The MOSFET switches SW1 and SW2 are turned on alternatively and are subjected to a voltage stress equal to that of the input voltage. Because the capacitors provide a mid-voltage point, the transformer sees a positive and negative voltage during switching. This results in twice the desired peak flux value of the core because the transformer core is operated in the first and third quadrants off the B-H loop, and it experiences twice the flux excursion of a similar forward-converter core.
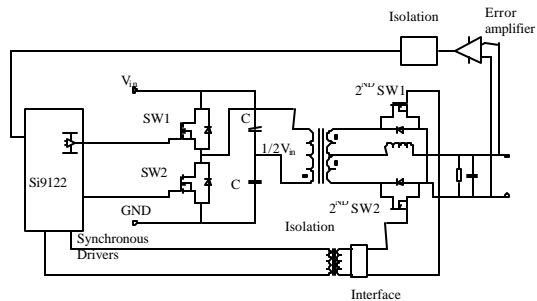
Figure 3. Schematic of the half-bridge dc-to-dc converter.[2]

The Forward Converter

The forward converter is very similar to the step-down dc-to-dc converter, with the transformer providing galvanic isolation and not being used to store energy. For the topology investigated in this paper, a simple reset winding is included to reset the magnetizing current in the transformer and prevent core saturation. The circuit used is a self-resonant reset circuit, which resets the magnetizing current and also recovers this magnetizing energy by charging it back to the input. This topology also allows for large ratio of input-to-output voltages.

The controller used is a Vishay Siliconix Si9118DY, and for simplicity the readily available 25-W demo baord[4] is used to evaluate a range of devices with varying parameters. Although the target requirement would be 100 W (from Table 1), the circuit investigated gives a valid comparison of switching devices. This demo board is used to determine the performance of two distributed buses, one with an output voltage of 12 V and another with an output voltage of 3.3 V. To obtain the 12-V output, the demo baord[3&4] was altered slightly. This included altering the number of turns on the transformer to 10 from 21, changing the feedback resistors, and using higher-voltage-output capacitors. The schematic of the circuit is shown in Figure 4. For the 3.3-V output, the only change to the demo board was to the feedback resistors.

Results: 12-V Output

Initially, two devices were chosen for the primary switch comparison, these being the Si9422DY and the Si4490DY. These gave a good trade-off between $r_{DS(on)}$ and gate charge (Q_g), with the Si9422DY having higher on-resistance and the Si4490DY having slower switching times. Table 3 shows the measured efficiencies of the converter using these two devices. It should be noted that the transformer has not been designed for the 12-V output – as this is beyond

the scope of this paper – and as such may contribute to higher losses than normally would be expected.
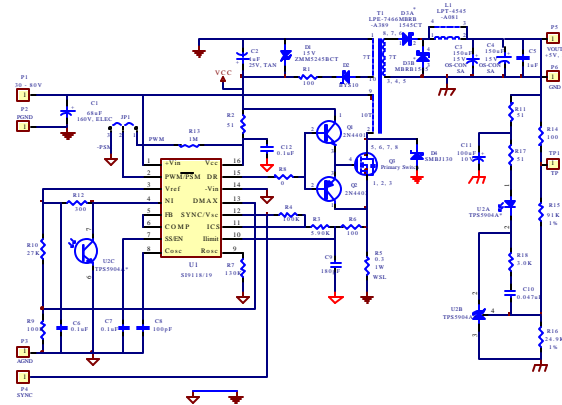
Figure 4. Schematic showing the circuit used to provide a 12-V, 2.5-A output.[3&4]

The results in Table 3 show that increasing the switching frequency from 500 kHz to 1 MHz increases the efficiency in some conditions by 6%. However, increasing the switching frequency of the converter increases the switching losses of the primary MOSFET. Therefore, the losses in the transformer, in this instance, must contribute more to the total losses of the converter than the MOSFET, as increasing the switching frequency reduces the energy requirement or size of the core.

Table 3 also shows that the converter operated with a lower input voltage of 36 V is more efficient than when it is operated with a higher input voltage of 48 V or 60 V. This demonstrates that the switching losses are the dominant factor in the primary device. Using the equations in Table 5 and the idealized waveforms in Figure 6, it can be shown that by decreasing the input voltage from 60 V to 36 V, the switching losses will increase by approximately 40%, whereas the increase in conduction losses (due to the I^2 relationship) is approximately 70%. Therefore, if the losses were equally distributed, then changing the input voltage would have more of an impact on the conduction losses. Because this is not the case, the switching losses must be considerably more than the conduction losses.

The efficiency results also show the trade-off between conduction losses and switching losses for the comparison of the two MOSFETs. At the higher current levels, the lower $r_{DS(on)}$ device becomes more efficient, especially at the lower input voltage where the current will also be larger (36 V_{in}, 2.5A, 1 MHz). However, at the slightly lower current levels (60 V_{in}, 1,5 A, 1MHz), the

higher $r_{DS(on)}$ device is more efficient. This is due to the fact that reducing the $r_{DS(on)}$ at higher load currents counteracts the penalty of increased switching losses associated with higher Q_g.

		Switching Frequency								
		500kHz			750kHz			1MHz		
		Load current [A]			Load current [A]			Load current [A]		
	DC input [V]	1.5	2	2.5	1.5	2	2.5	1.5	2	2.5
9 4 2 2	36	75	77	78	80	82	83	81	83	84
	48	70	75	76	75	78	81	76	79	81
	60	67	71	75	71	75	77	72	76	78
4 4 9 0	36	77	78	80	80	83	84	81	83	85
	48	71	75	77	75	79	81	76	80	80
	60	67	72	75	70	74	77	71	76	78

Table 3. Efficiency of the Si9118DY 12-V converter using two different MOSFETs as the primary switch.

Three more devices were added to the comparison, and the efficiency results are shown in Table 4. The best efficiencies are achieved with the 1-MHz switching frequencies and with the Si4848DY. Again, this shows that the major losses are associated with the transformer. To obtain lower losses, the switching frequency must be increased. However, it is the combination of the fast switching times and low $r_{DS(on)}$ of the Si4848DY that provides the most efficient converter for a 48-V input and 1-MHz switching frequency. However, at the lower switching frequencies, the part with even-lower $r_{DS(on)}$, the Si4488DY, is more efficient.

Device	V_{ds} [V]	$r_{ds(on)}$ max [Ω]	Q_g typ [nC]	500kHz	750kHz	1MHz
				Switching frequency		
Si9420DY	200V	1	8.6	72% @ 2A	76% @ 2A	77% @ 2A
Si9422DY	200V	0.42	13	76%	81%	81%
Si4490DY	200V	0.08	34	77%	81%	80%
Si4488DY	150V	0.05	30	78%	81%	80%
Si4848DY	150V	0.085	17	77%	81%	82%

Table 4. Efficiencies at 48-V input, 12-V output, and load current of 2.5 A.
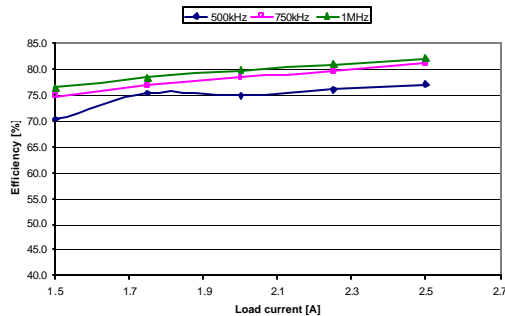
Figure 5. Efficiency for the 12-V converter, with 48-V input and with the Si4848DY MOSFET as the primary switch
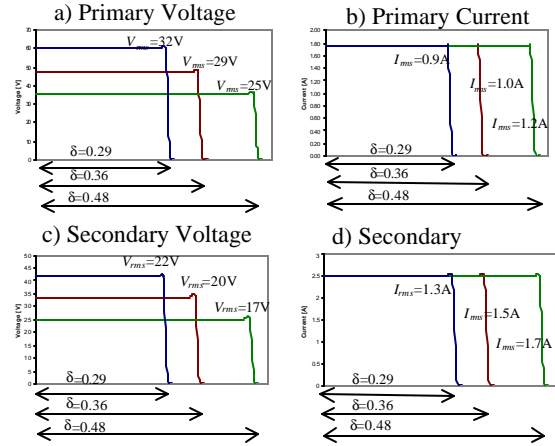
Figure 6. Idealized current and voltage waveforms for 12-V and 2.5-A output.
Key δ=0.29 Vin 60V; δ=0.36 Vin 48V; δ=0.48 Vin 32V

	Loss equations
Primary Switch	$P_{con} = R_{ds(on)} I^2 d$
	$P_{sw} = \frac{1}{2} VI(t_f + t_r)f_s$
	$P_{gate} = Q_g V_g f_{sw}$
D1	$P_{con} = V_{sat} I(d)$
D2	$P_{con} = V_{sat} I(1-d)$
D1+ D2	$P_{rr} = Vt_{rr}\left(\dfrac{I_{rr}}{2} + I\right)f_s$

Table 5. Generic loss equations for the active devices in a forward converter.

Results: 3.3-V Output

As with the example of the 12-V converter, two devices initially were chosen for the primary switch comparison. Table 6 shows the measured efficiencies of the converter using the Si9422DY and the Si4490DY.

The highest efficiency occurs at a load current of between 2 A and 3 A, a range that ties in with the efficiencies of the 12-V output converter and the demo baord[4], which also had their highest efficiencies at 2.5 A. The efficiency appears to be dependent on current rather than power throughput, which may be due to the losses in the secondary-side Schottky diodes.

With the 3.3-V converter, the efficiency does not always improve with a lower input voltage. This means that the trade-off between switching losses and conduction losses is not as definitive as it was in the 12-V output case. Figure 8 shows the current and voltage waveforms for the 3.3-V converter, and it is seen that even though the rms values of the voltage will be lower, the peak values of the voltage will be the same for the 3.3-V output converter as for the 12-V converter. The primary current peak will be higher for the 3.3-V

converter with the same power throughput, resulting in higher switching losses for the same power. The conduction losses will also be higher because the rms current is higher for the same output power. Therefore, the losses for the 3.3-V converter will be greater than those for the 12-V converter for a given power output. This is not necessarily the case in this paper, due to the dominance of the modified transformer in the 12-V converter.

Device [Freq]	Vin [V]	Efficiency [%] @ Load current [A]							
		1	2	3	4	5	6	7	8
9422DY [500kHz]	36	78	80	**81**	80	79	78	77	75
	48	77	**82**	81	80	80	79	78	76
	60	75	81	**82**	80	79	79	77	76
9422DY [750kHz]	36	76	**81**	79	79	78	77	76	74
	48	75	80	**82**	79	79	78	77	75
	60	73	80	**81**	81	78	78	77	75
9422DY [1MHz]	36	72	79	**81**	78	77	76	75	74
	48	71	78	**80**	80	77	77	76	74
	60	69	77	79	**80**	77	76	75	74
4490DY [500kHz]	36	75	78	**80**	80	80	79	78	77
	48	71	79	**79**	**79**	79	79	78	77
	60	69	78	**80**	78	79	78	78	76
4490DY [750kHz]	36	76	79	**80**	80	79	78	77	76
	48	68	76	79	**80**	78	77	77	76
	60	65	74	77	**78**	77	77	76	75
4490DY [1MHz]	36	-	-	-	-	-	-	-	-
	48	75	74	76	**76**	76	76	75	73
	60	61	72	75	**77**	77	75	75	74

Table 6. Efficiency of the Si9118DY 3.3-V converter using two different MOSFETS as the primary switch.

Again, as with the 12-V converter test, three more devices were added for comparison (Table 7). In these tests the most efficient circuit has a 750-kHz switching frequency, which means that the transformer losses are not dominant, as they were with the 12-V output converter. In the 3.3-V converter, it is obvious that the switching losses of the primary device dominate the losses because the Si9422DY, with the lowest Q_g, is the most efficient device. However, at the higher loads (8 A, 750 kHz), it is the combination of the low switching and $r_{DS(on)}$ of the Si4848DY that provides the most efficient converter with an efficiency measurement of 79%.

Device	V_{ds} [V]	$r_{ds(on)}$ max [W]	Q_g typ [nC]	Load [A]	Switching frequency [kHz]		
					500	750	1000
Si9420 DY	200V	1	8.6	3	-	80	78
				8	-	73 (@7)	67(@7)
Si9422 DY	200V	0.42	13	3	81	**82**	80
				8	76	75	74
Si4490 DY	200V	0.08	34	3	79	**79**	76
				8	77	76	73
Si4488 DY	150V	0.05	30	3	79	**77**	76
				8	77	76	74
Si4848 DY	150V	0.085	17	3	80	**79**	77
				8	73	77	75

Table 7. Efficiencies using five different primary switches with a 48-V input and 3.3-V output.
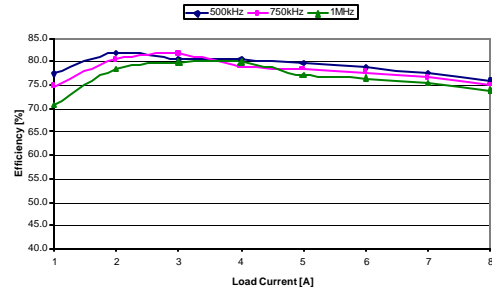
Figure 7. Efficiency for the 3.3-V converter
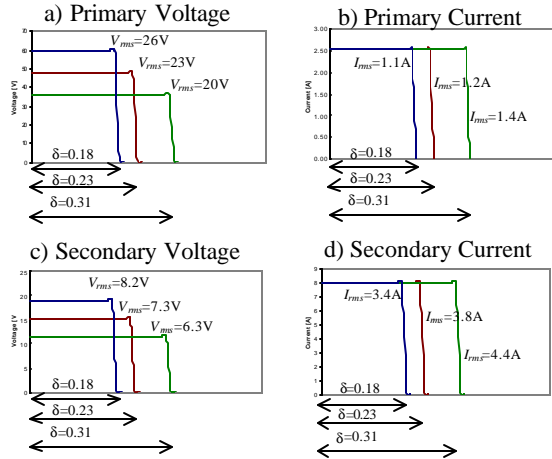
**Figure 8. Idealized current and voltage waveforms for 3.3 -V and 8 -A output.**
Key δ=0.18 Vin 60V; δ=0.23 Vin 48V; δ=0.31 Vin 32V
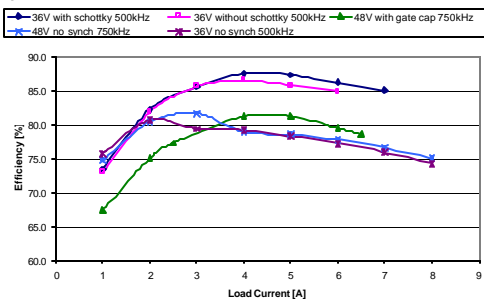
Secondary Synchronous Rectification
One of the factors that affects the efficiency of the 3.3-V converter at the higher load currents necessary to obtain the same power output is the IV losses in the rectifier diodes (D3A and D3B in Figure 4). Therefore, these diodes were can be replaced with MOSFETS to reduce conduction losses.

Self-driven secondary synchronous rectification is relatively simple to achieve with forward converters and is shown in Figure 9. However, care must be taken with the voltage levels that appear on the secondary-side transformer. For example, in considering the ideal voltage across the secondary transformer (Figure 8) for the 12-V converter, the minimum voltage is 25 V. However, with voltage overshoots this voltage often exceeds 30 V. Therefore, synchronous rectification was not considered for the 12-V converter due to the maximum gate-source voltages, which are typically 20 V. Furthermore, because the current levels in the 12-V converter are considerably lower than in the 3.3-V

converter, the benefits of introducing synchronous rectification are not as great.

With an input voltage of 36 V, the 3.3-V converter secondary-side voltage was below 20 V (the maximum gate source voltage allowed for these devices). Therefore, the Si4888DY, which offers a good combination of Q_g and $r_{DS(on)}$, was used as the MOSFET for synchronous rectification. For an input of 48-V, the secondary-side voltage reached values higher than 20 V, so a capacitor was used in series with the gate of the MOSFET. This reduces the gate source voltage appearing on the MOSFET, but it has the disadvantage of slowing the device and increasing the gate losses (Figure 10).

Another option is to use a Schottky diode in parallel with the synchronous MOSFET to improve the reverse recovery characteristics. An advantage of this method is that the Schottky can have a greatly reduced current capability, as it will only be conducting for a small amount of the time.
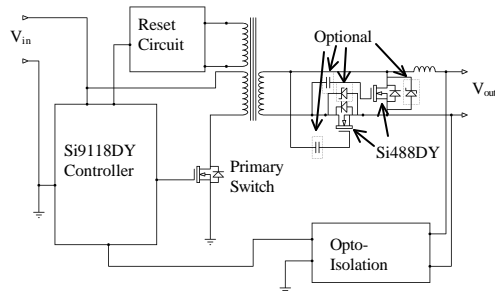
Figure 9. Schematic of the self-driven synchronous rectification.

Figure 10. Synchronous rectification with 3.3-V output.

The Point of Load Converter

Although not considered in detail in this paper, the actual point of load converter has several important characteristics. First, it does not need to be isolated because the front-end converter has achieved this. Second, depending on the required voltage levels, the POL converters can

be synchronous buck or synchronous boost to provide the greatest efficiency. Finally, the controllers can also be simple to allow for the smallest size.

For the MOSFET devices used for these synchronous converters, there are also desirable characteristics, such as shoot-through protection to prevent spurious turn-on of the low-side switch. This has come about due to the need for increased switching times and hence smaller dead-times. Also, for the synchronous MOSFET (lower-side switch in buck), the $r_{DS(on)}$ characteristics are more important, and with higher power levels, the packages are becoming more critical in increasing the power density.

Conclusion

These results have shown that it is very difficult to predict the performance of a MOSFET in a switching converter. In some circumstances the major factor contributing to losses may be the $r_{DS(on)}$, and for another load point, the switching transients will be more important. Therefore, in some circumstances it may be more desirable to fix the parameters of the converter by fixing the output current rather than the output voltage. With the need to bus an intermediate voltage around the board, the voltage regulation can be accounted for with the point of load converter. In this case, the distributed intermediate voltage does not necessarily need to be a fixed voltage.

Another issue is the requirement for the distributed bus voltage level. Lower voltage outputs mean higher load currents and more losses for the same power levels, but a 3.3-V distributed bus does have the advantage of having the 3.3-V output available when required. The efficiency can be improved dramatically with synchronous rectification, which may not be the case with the higher-output-voltage converter. Therefore, care must be taken in choosing the correct topology and MOSFET for a given application, and in some circumstances the devices and circuits should be chosen via practical testing.

References

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